WHAT IS CLAIMED IS:

1. A transistor comprising:
an n-type well in a drain side of a p-type substrate;
an n+-type drain diffusion region in the well;
a p-type halo in a source side of the substrate;
an n-type lightly doped drain in the halo; and
an n+-type source diffusion region in the lightly doped drain.

2. The transistor of claim 1, further comprising:
a drain terminal connected to the drain diffusion region;
a source terminal connected to the source diffusion region;
a layer of gate dielectric over the substrate between the drain diffusion region and the source diffusion region;
a polysilicon gate over the layer of gate dielectric;
an electrode over the polysilicon gate;
a spacer on sides of the gate dielectric, the polysilicon gate, and the electrode; and
a gate terminal connected to the electrode.

3. A method of forming a transistor comprising:
forming an n-type well in a drain side of a p-type substrate;
forming an n+-type drain diffusion region in the well;
forming a p-type halo in a source side of the substrate;
forming an n-type lightly doped drain in the halo; and
forming an n+-type source diffusion region in the lightly doped drain.

4. The method of claim 3, further comprising:
connecting a drain terminal to the drain diffusion region;
connecting a source terminal to the source diffusion region;

forming a layer of gate dielectric over the substrate between the drain diffusion region and the source diffusion region;

forming a polysilicon gate over the layer of gate dielectric;

forming an electrode over the polysilicon gate;

forming a spacer on sides of the gate dielectric, the polysilicon gate, and the electrode; and

connecting a gate terminal to the electrode.

5. A transistor comprising:

a p-type halo in a source side of a p-type substrate;

an n-type lightly doped drain in the halo;

an n+-type source diffusion region in the lightly doped drain; and

an n+-type drain diffusion region in a drain side of the substrate.

6. The transistor of claim 5, further comprising:

a drain terminal connected to the drain diffusion region;

a source terminal connected to the source diffusion region;

a layer of gate dielectric over the substrate between the drain diffusion region and the source diffusion region;

a polysilicon gate over the layer of gate dielectric;

an electrode over the polysilicon gate;

a spacer on sides of the gate dielectric, the polysilicon gate, and the electrode; and

a gate terminal connected to the electrode.

7. A method of forming a transistor comprising:

forming a p-type halo in a source side of a p-type substrate;

forming an n-type lightly doped drain in the halo;

forming an n+-type source diffusion region in the lightly doped drain; and

forming an n+-type drain diffusion region in a drain side of the substrate.

8. The method of claim 7, further comprising:

connecting a drain terminal to the drain diffusion region;

connecting a source terminal to the source diffusion region;

forming a layer of gate dielectric over the substrate between the drain diffusion region and the source diffusion region;

forming a polysilicon gate over the layer of gate dielectric;

forming an electrode over the polysilicon gate;

forming a spacer on sides of the gate dielectric, the polysilicon gate, and the electrode; and

connecting a gate terminal to the electrode.

9. An integrated circuit comprising:

an external pin;

a common bus line coupled to the external pin;

an antifuse bank coupled to the common bus line, the antifuse bank comprising a plurality of antifuses; and

a common bus line driver circuit comprising:

a high-voltage transistor having a first terminal coupled to the common bus line, a control terminal, and a second terminal;

a diode coupled between the control terminal and a reference voltage; and

a control transistor coupled between the second terminal and a voltage reference.

10. The integrated circuit of claim 9 wherein:

the high-voltage transistor comprises an n-well drain transistor having a drain terminal coupled to the common bus line, a control terminal coupled to the diode, and a source terminal coupled to the control transistor;

the diode comprises:

a first diode comprising an anode coupled to a voltage supply and a cathode coupled to the control terminal of the n-well drain transistor; and

a second diode comprising an cathode coupled to the control terminal of the n-well drain transistor and an anode coupled to a voltage reference to withstand a high voltage on the control terminal of the n-well drain transistor;

the control transistor is coupled between the second terminal and a reference voltage and further comprises a control circuit to switch on the control transistor to couple the common bus line to the ground voltage reference and to switch off the control transistor to permit an elevated voltage on the common bus line.

11. A method of operating an integrated circuit comprising:

coupling an elevated voltage through an external pin to a common bus line in the integrated circuit to program an antifuse coupled to the common bus line;

switching off a control transistor in a common bus line driver circuit coupled between the common bus line and a voltage reference to substantially prevent current flow from the common bus line;

bearing a portion of the elevated voltage across a high-voltage transistor having a first terminal coupled to the common bus line, a control terminal, and a second terminal coupled to the control transistor;

bearing a portion of the elevated voltage between a diode and the control terminal of the high-voltage transistor; and

switching on the control transistor to couple the common bus line to the voltage reference to read the antifuse.

12. The method of claim 11 wherein:

switching off a control transistor comprises switching off a control transistor with a control circuit in a common bus line driver circuit coupled between the common bus line and a voltage reference to substantially prevent current flow from the common bus line;

bearing a portion of the elevated voltage across a high-voltage transistor comprises bearing a portion of the elevated voltage across an n-well drain transistor having a drain terminal coupled to the common bus line, a control terminal coupled to a diode, and a source terminal coupled to the control transistor;

bearing a portion of the elevated voltage between a diode and the control terminal comprises bearing a portion of the elevated voltage between the control terminal of the n-well drain transistor, a first diode comprising an anode coupled to a voltage supply and a cathode coupled to the control terminal of the n-well drain transistor, and a second diode comprising a cathode coupled to the control terminal of the n-well drain transistor and an anode coupled to a reference voltage; and

switching on the control transistor comprises switching on the control transistor with the control circuit to couple the common bus line to the voltage reference to read the antifuse.

13. A circuit comprising:

a high-voltage transistor comprising:

a well of a first conductivity type in a substrate of a second conductivity type;

a drain diffusion region of the first conductivity type in the well, the drain diffusion region being coupled to an elevated voltage source;

a source diffusion region of the first conductivity type in the substrate;

a layer of gate dielectric over the substrate; and --

a gate electrode over the gate dielectric;

a diode coupled between the gate electrode and a reference voltage to hold a voltage on the gate electrode caused by a charge transfer across the gate dielectric due to the elevated voltage source;

a support circuit coupled to the source diffusion region.

14. The circuit of claim 13 wherein:

the substrate comprises a p-type substrate;

the well comprises an n-type well in the p-type substrate;

the drain diffusion region comprises an n+-type drain diffusion region in the n-type well;

the source diffusion region comprises an n+-type source diffusion region in the p-type substrate;

the gate dielectric comprises a layer of oxide;

the gate electrode comprises a gate electrode over the layer of oxide;

the diode comprises:

a first diode comprising an anode coupled to a voltage supply and a cathode coupled to the gate electrode of the high-voltage transistor to switch on the high-voltage transistor; and

a second diode comprising a cathode coupled to the gate electrode of the high-voltage transistor and an anode coupled to a reference voltage to withstand a high voltage on the gate electrode; and

the support circuit comprises a control transistor is coupled between the source diffusion region and a ground voltage reference and further comprises a control circuit to switch on the control transistor to couple the elevated voltage source to the ground voltage reference and to switch off the control transistor to permit the circuit to bear the elevated voltage.

15. A method comprising:

coupling an elevated voltage to a drain of a high-voltage transistor;

allowing charge to transfer from the drain across a layer of gate dielectric to a gate electrode of the high-voltage transistor; and

allowing the charge to accumulate in the gate electrode to raise a voltage of the gate electrode to a balanced voltage to reduce further charge transfer across the layer of gate dielectric.

16. The method of claim 15 wherein:

coupling an elevated voltage to a drain comprises coupling an elevated voltage to an n+-type drain diffusion region in an n-type well in a p-type substrate of a high-voltage transistor;

allowing charge to transfer from the drain comprises allowing charge to transfer from the n+-type drain diffusion region across a layer of gate oxide to a gate electrode of the high-voltage transistor; and

allowing the charge to accumulate comprises holding the charge in the gate electrode with a first diode comprising an anode coupled to a voltage supply and a cathode coupled to the gate electrode and a second diode comprising an cathode coupled to the gate electrode and an anode coupled to a reference voltage to raise a voltage of the gate electrode to a balanced voltage to reduce further charge transfer across the layer of oxide.

17. An antifuse circuit comprising:

an antifuse having a first terminal coupled to a programming voltage supply and a second terminal;

a high-voltage transistor comprising:

a well of a first conductivity type in a substrate of a second conductivity type;

a drain diffusion region of the first conductivity type in the well, the drain diffusion region being coupled to the second terminal of the antifuse;

a source diffusion region of the first conductivity type in the substrate;

a layer of gate dielectric over the substrate; and

a gate electrode over the gate dielectric;

a diode coupled between the gate electrode and a first reference voltage to hold a voltage on the gate electrode caused by a charge transfer across the gate dielectric due to the programming voltage;

an impedance transistor having a first terminal coupled to the source diffusion region of the antifuse and a second terminal; and

a control transistor having a first terminal coupled to the second terminal of the impedance transistor, a second terminal coupled to a second reference voltage, and a control terminal coupled to a control circuit to switch the control transistor on to couple the second terminal of the antifuse to the second reference voltage to program the antifuse, and to switch the control transistor off when the antifuse is not being programmed.

18. The antifuse circuit of claim 17 wherein:

the substrate comprises a p-type substrate;

the well comprises an n-type well in the p-type substrate;

the drain diffusion region comprises an n+-type drain diffusion region in the n-type well;

the source diffusion region comprises an n+-type source diffusion region in the p-type substrate;

the gate dielectric comprises a layer of oxide;

the gate electrode comprises a gate electrode over the layer of oxide;

the diode comprises:

a first diode comprising an anode coupled to a voltage supply and a cathode coupled to the gate electrode of the high-voltage transistor to switch on the high-voltage transistor; and

a second diode comprising a cathode coupled to the gate electrode of the high-voltage transistor and an anode coupled to a reference voltage to withstand a high voltage on the gate electrode;

the control transistor comprises an n-channel transistor; and

the impedance transistor comprises an n-channel transistor including a gate terminal coupled to the voltage supply.

19. A method of operating an antifuse circuit comprising:

coupling an elevated voltage to a first terminal of an antifuse from a common bus line;

coupling a second terminal of the antifuse to a reference voltage through a control transistor to program the antifuse with current from the common bus line;

switching off the control transistor to uncouple the second terminal of the antifuse from the reference voltage after the antifuse is programmed; and

reducing a voltage on a terminal of the control transistor with an impedance transistor coupled between the second terminal of the antifuse and the terminal of the control transistor to reduce a probability of snap-back in the control transistor.

20. The method of claim 19 wherein:

coupling an elevated voltage comprises coupling an elevated voltage from an external pin to a first terminal of an antifuse through a common bus line;

coupling a second terminal of the antifuse comprises coupling a second terminal of the antifuse to a ground reference voltage through an n-channel control transistor to program the antifuse with current from the common bus line;

switching off the control transistor comprises switching off the n-channel control transistor with a control circuit to uncouple the second terminal of the antifuse from the ground reference voltage after the antifuse is programmed; and

reducing a voltage comprises reducing a voltage on a drain terminal of the n-channel control transistor with an n-channel impedance transistor that is switched on and coupled between the second terminal of the antifuse and the drain terminal of the control transistor to reduce a probability of snap-back in the control transistor.

21. A method of operating an antifuse circuit comprising:

coupling an elevated voltage to a first terminal of an unprogrammed antifuse from a common bus line;

separating a second terminal of the antifuse from a reference voltage with a control transistor that is switched off; and

reducing a voltage on a terminal of the control transistor with an impedance transistor coupled between the second terminal of the antifuse and the terminal of the control transistor to reduce leakage current in the control transistor.

22. The method of claim 21 wherein:

coupling an elevated voltage comprises coupling an elevated voltage from an external pin to a first terminal of an antifuse through a common bus line;

separating a second terminal of the antifuse comprises separating a second terminal of the antifuse from a ground reference voltage with an n-channel control transistor that is switched off; and

reducing a voltage comprises reducing a voltage on a drain terminal of the n-channel control transistor with an n-channel impedance transistor that is switched on and coupled between the second terminal of the antifuse and the drain terminal of the control transistor to reduce leakage current in the control transistor.

23. An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising:

a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse in an active mode; and

a latch circuit to latch a state of the antifuse in a sleep mode.

24. The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference; and the transistor comprises a p-channel transistor having a source terminal coupled to the read voltage and a gate terminal coupled to a bias voltage;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors.

25. A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a transistor;

detecting a voltage of the second terminal of the antifuse to read the antifuse in an active mode; and

latching the voltage of the second terminal of the antifuse in a sleep mode.

26. The method of claim 25 wherein:

coupling a reference voltage comprises coupling a ground reference voltage to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel transistor switched on by a bias voltage;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter in an active mode; and

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter in a sleep mode. --

27. An antifuse circuit comprising:

an antifuse having a first terminal coupled to an elevated voltage in a programming mode and a reference voltage in an active mode;

a read circuit comprising a p-channel transistor coupled between a read voltage source and a second terminal of the antifuse to couple the read voltage source to the antifuse to read the antifuse in the active mode; and a floating well driver logic circuit coupled to a gate terminal and a well of the p-channel transistor to raise a voltage of the gate terminal and the well in the programming mode to substantially prevent current in the p-channel transistor.

28. The antifuse circuit of claim 27 wherein:

the antifuse comprises an antifuse having a first terminal coupled to a common bus line, the common bus line being coupled to the elevated voltage in the programming mode and to a ground reference voltage in the active mode;

the read circuit further comprises a plurality of p-channel transistors, one of the p-channel transistors being coupled between the second terminal of the antifuse and the floating well driver logic circuit to couple a rising voltage on the second terminal of the antifuse to the floating well driver logic circuit; and

the floating well driver logic circuit further comprises a voltage source coupled to a gate terminal and a well of selected ones of the p-channel transistors in the read circuit to raise a voltage of the gate terminals and the wells in the programming mode to substantially prevent current in the selected p-channel transistors.

29. A method of operating an antifuse circuit, comprising:

coupling an elevated voltage to a first terminal of an antifuse in a programming mode and coupling a reference voltage to the first terminal in an active mode;

reading the antifuse in the active mode with a p-channel transistor coupled between a read voltage source and a second terminal of the antifuse; and

raising a voltage of a gate terminal and a well of the p-channel transistor in the programming mode to substantially prevent current in the p-channel transistor.

30. The method of claim 29 wherein:

coupling a reference voltage comprises coupling a ground reference voltage to the first terminal in the active mode;

reading the antifuse further comprises:

coupling the read voltage source to the second terminal of the antifuse; and

detecting a voltage on the second terminal of the antifuse with an inverter in a read circuit; and

raising a voltage comprises:

coupling a rising voltage on the second terminal of the antifuse to a gate terminal and a well of each of a plurality of p-channel transistors in the read circuit.

31. An integrated circuit comprising:

an external pin coupled to a common bus line to couple an elevated voltage to an antifuse having a first terminal coupled to the common bus line to program the antifuse in a programming mode;

a program driver circuit coupled to a second terminal of the antifuse to select the antifuse to be programmed in the programming mode;

a common bus line driver circuit to couple the common bus line to a reference voltage during an active mode;

a read circuit coupled to the second terminal of the antifuse to read the antifuse during the active mode;

a latch circuit coupled to the second terminal of the antifuse to latch a state of the antifuse during a sleep mode; and

a floating well driver logic circuit coupled to the read circuit and the latch circuit to switch off transistors in the read circuit and the latch circuit during the programming mode.

32. An integrated memory device comprising:

an array of memory cells;

an address decoder;

a plurality of input/output paths;

an input/output control circuit; and

an antifuse circuit comprising:

an external pin coupled to a common bus line to couple an elevated voltage to an antifuse having a first terminal coupled to the common bus line to program the antifuse in a programming mode;

a program driver circuit coupled to a second terminal of the antifuse to select the antifuse to be programmed in the programming mode;

a common bus line driver circuit to couple the common bus line to a reference voltage during an active mode;

a read circuit coupled to the second terminal of the antifuse to read the antifuse during the active mode;

a latch circuit coupled to the second terminal of the antifuse to latch a state of the antifuse during a sleep mode; and

a floating well driver logic circuit coupled to the read circuit and the latch circuit to switch off transistors in the read circuit and the latch circuit during the programming mode.

33. An integrated circuit comprising:

an external pin coupled to a common bus line to couple an elevated voltage to an antifuse having a first terminal coupled to the common bus line to program the antifuse in a programming mode;

a program driver circuit coupled to a second terminal of the antifuse to select the antifuse to be programmed in the programming mode;

a common bus line driver circuit to couple the common bus line to a reference voltage during an active mode;

means for reading the antifuse during the active mode;

a latch circuit coupled to the second terminal of the antifuse to latch a state of the antifuse during a sleep mode; and

means for switching off transistors in the read circuit and the latch circuit during the programming mode.

34. The antifuse circuit of claim 23 wherein:

the read transistor comprises a p-channel read transistor having a source terminal coupled to the read voltage and a gate terminal coupled to a bias voltage;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising a p-channel transistor coupled between the read transistor and the second terminal of the antifuse that is switched on when the antifuse is being read.

35. The antifuse circuit of claim 23, further comprising:

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode;

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference;

a floating well driver logic circuit coupled to a gate terminal and a well of a p-channel transistor in the read circuit or the latch circuit to raise a voltage of the gate terminal and the well during the programming mode to substantially prevent current in the p-channel transistor; and

wherein the read circuit further comprises a plurality of p-channel transistors, one of the p-channel transistors being coupled between the second terminal of the antifuse and the floating well driver logic circuit to couple a rising voltage on the second terminal of the antifuse to the floating well driver logic circuit.

36. The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises an n-channel transistor having a drain terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a source terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of n-channel latch circuit transistors and an output coupled to gate terminals of the n-channel latch circuit transistors; and

further comprising an n-channel transistor coupled between the read transistor and the second terminal of the antifuse that is switched on when the antifuse is being read.

37. The antifuse circuit of claim 23 wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

38. The antifuse circuit of claim 23 wherein:

the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising n-type material, the first terminal being coupled to a voltage source;

the read transistor comprises a long-L n-channel transistor having a source terminal coupled to a ground voltage reference, a gate terminal coupled to a bias voltage, and a drain terminal coupled to the second terminal of the antifuse; and

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors.

39. The method of claim 25 wherein:

coupling a read voltage further comprises coupling the read voltage to the second terminal of the antifuse through a p-channel read transistor switched on by a bias voltage during the active mode;

detecting a voltage further comprises detecting the voltage of the second terminal of the antifuse with an input of an inverter during the active mode;

latching the voltage further comprises latching the voltage of the second terminal of the antifuse with a latch circuit comprising the inverter coupled to a plurality of latch transistors; and

further comprising switching on a p-channel transistor coupled between the read transistor and the second terminal of the antifuse during the active mode.

40. The method of claim 25, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode;

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse; and

switching off transistors in a read circuit coupled to the antifuse during the programming mode with a floating well driver logic circuit coupled to the read circuit by raising a voltage of a gate terminal and a well of a p-channel transistor to substantially prevent current in the p-channel transistor.

41. The method of claim 25 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode; and latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of n-channel latch transistors during a sleep mode.

42. The method of claim 25 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

43. The method of claim 25 wherein:

coupling a reference voltage comprises coupling a voltage source to a first terminal of an antifuse, the first terminal comprising n-type material;

coupling a read voltage comprises coupling a ground voltage reference to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage, the second terminal comprising n-type material;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter; and

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch circuit transistors.

44. An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal; and

a read circuit to read the antifuse, the read circuit comprising a transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse.

45. The antifuse circuit of claim 44 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the transistor comprises a p-channel transistor having a source terminal coupled to the read voltage and a gate terminal coupled to a bias voltage; and

the read circuit further comprises an inverter having an input coupled to the second terminal of the antifuse.

46. The antifuse circuit of claim 44, further comprising:

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode;

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference;

a floating well driver logic circuit coupled to a well of a p-channel transistor in the read circuit to raise a voltage of the well during the programming mode to substantially prevent current in the p-channel transistor; and

wherein the read circuit further comprises a plurality of p-channel transistors, one of the p-channel transistors being coupled between the second terminal of the antifuse and the floating well driver logic circuit to couple a rising voltage on the second terminal of the antifuse to the floating well driver logic circuit.

47. The antifuse circuit of claim 44 wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

48. A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a transistor; and

detecting a voltage of the second terminal of the antifuse to read the antifuse.

49. The method of claim 48 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel transistor switched on by a bias voltage; and

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter.

50. The method of claim 48, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode;

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse; and

switching off a p-channel transistor in a read circuit coupled to the antifuse during the programming mode with a floating well driver logic circuit coupled to the read circuit by raising a voltage of a well of the p-channel transistor to substantially prevent current in the p-channel transistor.

51. The method of claim 48 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

52. An antifuse circuit comprising:

an antifuse having a first terminal coupled to a reference voltage and a second terminal;

a read circuit to read the antifuse, the read circuit comprising:

a read transistor coupled between a read voltage and the antifuse to couple the read voltage to the antifuse to read the antifuse during an active mode; and

a latch circuit to latch a state of the antifuse during a sleep mode; and

a pass-gate device coupled between the antifuse and the read circuit.

53. The antifuse circuit of claim 52 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises a p-channel transistor having a source terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a drain terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising a p-channel transistor coupled between the read transistor and the pass gate device that is switched on when the antifuse is being read.

54. The antifuse circuit of claim 52 wherein:

the antifuse comprises a gate dielectric between the first terminal and the second terminal, the first terminal being coupled to a ground voltage reference;

the read transistor comprises an n-channel transistor having a drain terminal coupled to the read voltage, a gate terminal coupled to a bias voltage, and a source terminal coupled to the second terminal of the antifuse;

the latch circuit comprises an inverter having an input coupled to the second terminal of the antifuse and to a plurality of latch circuit transistors and an output coupled to gate terminals of the latch circuit transistors; and

further comprising an n-channel transistor coupled between the read transistor and the pass gate device that is switched on when the antifuse is being read.

55. The antifuse circuit of claim 52 wherein the antifuse comprises a gate dielectric between the first terminal comprising n-type material and the second terminal comprising p-type material, the first terminal being coupled to a ground voltage reference and the second terminal being coupled to the read circuit.

56. The antifuse circuit of claim 52 wherein the pass-gate device comprises an n-channel pass-gate transistor comprising a gate coupled to the read voltage.

57. The antifuse circuit of claim 52 wherein the pass-gate device comprises an n-channel pass-gate transistor comprising a gate coupled to a voltage different from the read voltage.

58. The antifuse circuit of claim 52, further comprising:

an external pin coupled to a common bus line to couple an elevated voltage to the first terminal of the antifuse to program the antifuse during a programming mode; and

a program driver circuit coupled to the second terminal of the antifuse to select the antifuse to be programmed during the programming mode, the program driver circuit comprising a high-voltage transistor and a control transistor coupled in series between the second terminal of the antifuse and a ground voltage reference.

59. A method of operating an antifuse circuit comprising:

coupling a reference voltage to a first terminal of an antifuse;

coupling a read voltage to a second terminal of the antifuse through a read transistor and a pass-gate device;

detecting a voltage of the second terminal of the antifuse to read the antifuse during an active mode; and

latching the voltage of the second terminal of the antifuse during a sleep mode.

60. The method of claim 59 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through a p-channel read transistor switched on by a bias voltage and a pass-gate device;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode;

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch transistors during a sleep mode; and

further comprising switching on a p-channel transistor coupled between the read transistor and the pass gate device during the active mode.

61. The method of claim 59 wherein:

coupling a reference voltage comprises coupling a ground voltage reference to a first terminal of an antifuse;

coupling a read voltage comprises coupling a read voltage to a second terminal of the antifuse through an n-channel read transistor switched on by a bias voltage and a pass-gate device;

detecting a voltage comprises detecting a voltage of the second terminal of the antifuse with an input of an inverter during an active mode;

latching the voltage comprises latching the voltage of the second terminal of the antifuse with a latch circuit including the inverter coupled to a plurality of latch transistors during a sleep mode; and

further comprising switching on an n-channel transistor coupled between the read transistor and the pass gate device during the active mode.

62. The method of claim 59, further comprising controlling current flow between the antifuse and the read transistor with the pass-gate device, the pass-gate device comprising an n-channel pass-gate transistor comprising a gate coupled to the read voltage.

63. The method of claim 59, further comprising controlling current flow between the antifuse and the read transistor with the pass-gate device, the pass-gate device comprising an n-channel pass-gate transistor comprising a gate coupled to a voltage different from the read voltage.

64. The method of claim 59 wherein:

coupling a reference voltage to a first terminal of an antifuse further comprises coupling the reference voltage to the first terminal comprising n-type material; and

coupling a read voltage to a second terminal of the antifuse further comprises coupling the read voltage to the second terminal of the antifuse comprising p-type material, the second terminal of the antifuse being separated from the first terminal of the antifuse by a gate dielectric.

65. The method of claim 59, further comprising:

coupling an elevated voltage to an external pin coupled to a common bus line and the first terminal of the antifuse to program the antifuse with the elevated voltage during a programming mode; and

switching on a control transistor coupled in series with a high-voltage transistor between the second terminal of the antifuse and a ground voltage reference to select the antifuse to be programmed during the programming mode, the antifuse comprising a gate dielectric between the first terminal and the second terminal of the antifuse.

66. An integrated circuit comprising:

an antifuse having a first terminal coupled to a common bus line;

a program driver circuit coupled to a second terminal of the antifuse to select the antifuse to be programmed during a programming mode;

means for reading the antifuse during an active mode; and

a latch circuit coupled to the second terminal of the antifuse to latch a state of the antifuse during a sleep mode.